QSFP-DD 400GBASE LR8 1310nm 10KM Transceiver

P/N: AE-QSFPDD-LR8

Features

- Compliant with IEEE 802.3bs standard:
  -400GBASE-LR8 optical interface
  -400GAU1-8 electricalinterface
- Compliant with QSFP-DD MSA HW Rev 3.0with duplex LC connector
- Maximum power consumption tbd W
- Case operating temperature 0° C to 70°C
- Two wire serial Interface with digital diagnostic monitoring
- Complies with EU Directive2011/65/EU (RoHS compliant)
- Class 1 Laser

Application

- 400GBASE-LR8 400G Ethernet
- Data Center

Product Specification

1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	Ts	-40	85	°C	
Supply Voltage	Vcc	-0.5	3.6	V	
Relative Humidity (non-condensing)	RH	5	95	%	
Data Input Voltage Differential	IV_{DIP}-$V_{DIN}I$		1	V	
Control input Voltage	V_I	-0.3	Vcc+0.5	V	
Control Output Current	I_0	-20	20	Ma	

2. Recommended Operating Environment

Parameter	Symbol	Min	TyP.	Max	Unit	Notes
Operating Case Temperature	T_{OPR}	0		70	°C	
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Instantaneous peak current at hotplug	I_{CC_IP}			TBD	mA	
Sustained peak current at hot plug	I_{CC_SP}			TBD	mA	
Maximum Power Dissipation	P_D			TBD	W	
Maximum Power Dissipation, LowPower Mode	P_{DLP}			TBD	W	
Signalling Speed per Lane	DRL		26.5625		Gbd	

Control input Voltage High	V_{IH}	V_{CC}*0.7		V_{CC}+0.3	V	
Control input Voltage Low	V_{IL}	-0.3		V_{CC}*0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise				50	mVpp	
Rx Differential Data Qutput Load			100		ohm	
Operating Distance		2		10000	m	

3. Optical Characteristics

The following tables list the performance specifications for the various functional blocks of the integrated optical transceiver module.

Parameter	Symbol	Min	TyP	Max	Unit	Notes
Transmitter						
Wavelength L0	λ_{C0}	1272.55	1273.55	1274.54	nm	
Wavelength L1	λ_{C1}	1276.89	1277.89	1278.89	nm	
Wavelength L2	λ_{C2}	1281.25	1282.26	1283.27	nm	
Wavelength L3	λ_{C3}	1285.65	1286.67	1287.68	nm	
Wavelength L4	λ_{C4}	1294.53	1295.56	1296.59	nm	
Wavelength L5	λ_{C5}	1299.02	1300.06	1301.09	nm	
Wavelength L6	λ_{C6}	1303.54	1304.59	1305.63	nm	
Wavelength L7	λ_{C7}	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	AOP_T			13.2	dBm	
Average Launch Power, each lane	AOP_L	-2.8		5.3	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}), each Lane	T_{OMA}	0.2		5.7	dBm	
Difference in Launch Power between any two Lanes (OMA_{outer})	D_{T_OMA}			4	dB	
Launch Power in OMA_{outer} minus TDECQ, each lane for ER> 4.5dB	$T_{OMA-TDECQ}$	-1.2			dBm	
Launch Power in OMA_{outer} minus TDECQ，each lane for ER< 4.5dB	$T_{OMA-TDECQ}$	-1.1			dBm	
Transmitter and Dispersion Eye Closure for PAM4(TDECQ), each lane	TDECQ			3.3	dB	

Average Launch Power of OFF Transmitter, each lane	T_{OFF}			-30	dBm	
Extinction Ratio	ER	3.5			dB	
$RIN_{15.1}OMA$	RIN			-132	dB/Hz	
Optical Return Loss Tolerance	ORL			15.1	dB	
Transmitter Reflectance	T_R			-26	dB	2

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength
2. Transmitter reflectance is defined looking into the transmitter

Parameter	**Symbol**	**Min**	**TyP**	**Max**	**Unit**	**Notes**
Receiver						
Wavelength L0	λ_{C0}	1272.55	1273.55	1274.54	nm	
Wavelength L1	λ_{C1}	1276.89	1277.89	1278.89	nm	
Wavelength L2	λ_{C2}	1281.25	1282.26	1283.27	nm	
Wavelength L3	λ_{C3}	1285.65	1286.67	1287.68	nm	
Wavelength L4	λ_{C4}	1294.53	1295.56	1296.59	nm	
Wavelength L5	λ_{C5}	1299.02	1300.06	1301.09	nm	
Wavelength L6	λ_{C6}	1303.54	1304.59	1305.63	nm	
Wavelength L7	λ_{C7}	1308.09	1309.14	1310.19	nm	
Damage Threshold, each Lane	AOP_D	6.3			dBm	
Average Receive Power, each Lane	AOP_R	-9.1		5.3	dBm	
Receive Power (OMA_{outer}), each Lane	OMA_R			5.7	dBm	
Difference in Receive Power between any two Lanes (OMA_{outer})	D_{R_OMA}			4.5	dB	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA_{outer}), each Lane	S_{OMA}			-7.1	dBm	1
Stressed Receiver Sensitivity (OMA_{outer}), each Lane	SRS			-4.7	dBm	2

Notes:

1. Receiver sensitivity (0MAouter, each lane (max) is informative and is defined for a transmitter with SECQ of 0.9 dB
2. Measured with conformance test signal at TP3 for the BER = $2.4x10^{-4}$

Electrical Characteristics

Table 1 - Electrical Specification High Speed Signal (compliant with IEEE 802.3bs 400GAU-8)

Parameter	Symbol	Min	TyP	Max	Unit	Notes
Transmitter (Module input)						
Differential pk-pk input Voltage tolerance		900			mV	
Differential termination mismatch				10	%	
Single-ended voltage tolerance range		-0.4		3.3	V	
DC common mode Voltage		-350		2850	mV	
Receiver (Module Output)						
AC common-mode output Voltage (RMS)				17.5	mV	
Differential output Voltage				900	mV	
Near-end Eye height, differential		70			UI	
Far-end Eye height, differential		30			UI	
Far end pre-cursor ratio				2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (min, 20% to 80%)		9.5			ps	
DC common mode Voltage		-350		2850	mV	

Table 2 - Electrical Specification Low Speed Signal (compliant with QSFP-DD HW Rev 3.0)

Parameter	Symbol	Min	Max	Unit	Condition
Module output SCL and SDA	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	
Module input SCL and SDA	V_{IL}	-0.3	V_{CC}*0.3	V	
	V_{IH}	V_{CC}*0.7	V_{CC}+0.5	V	
InitMode, ResetL and ModSelL	V_{IL}	-0.3	0.8	V	
	V_{IH}	2	V_{CC}+0.3	V	
IntL	V_{OL}	0	0.4	V	
	V_{OH}	V_{CC}-0.5	V_{CC}+0.3	V	

Digital Diagnostic Monitoring Information

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	°C	Internal
Voltage	0 to V_{CC}	0.1	V	Internal
Tx Bias Current (Each Lane)	0 to 100	10%	mA	Internal
Tx Output Power (Each Lane)	-3.5 to +5.3	±3dB	dBm	Internal
Rx Receive Power (Each Lane)	-9.1 to +5.3	±3dB	dBm	Internal

Pin Definitions

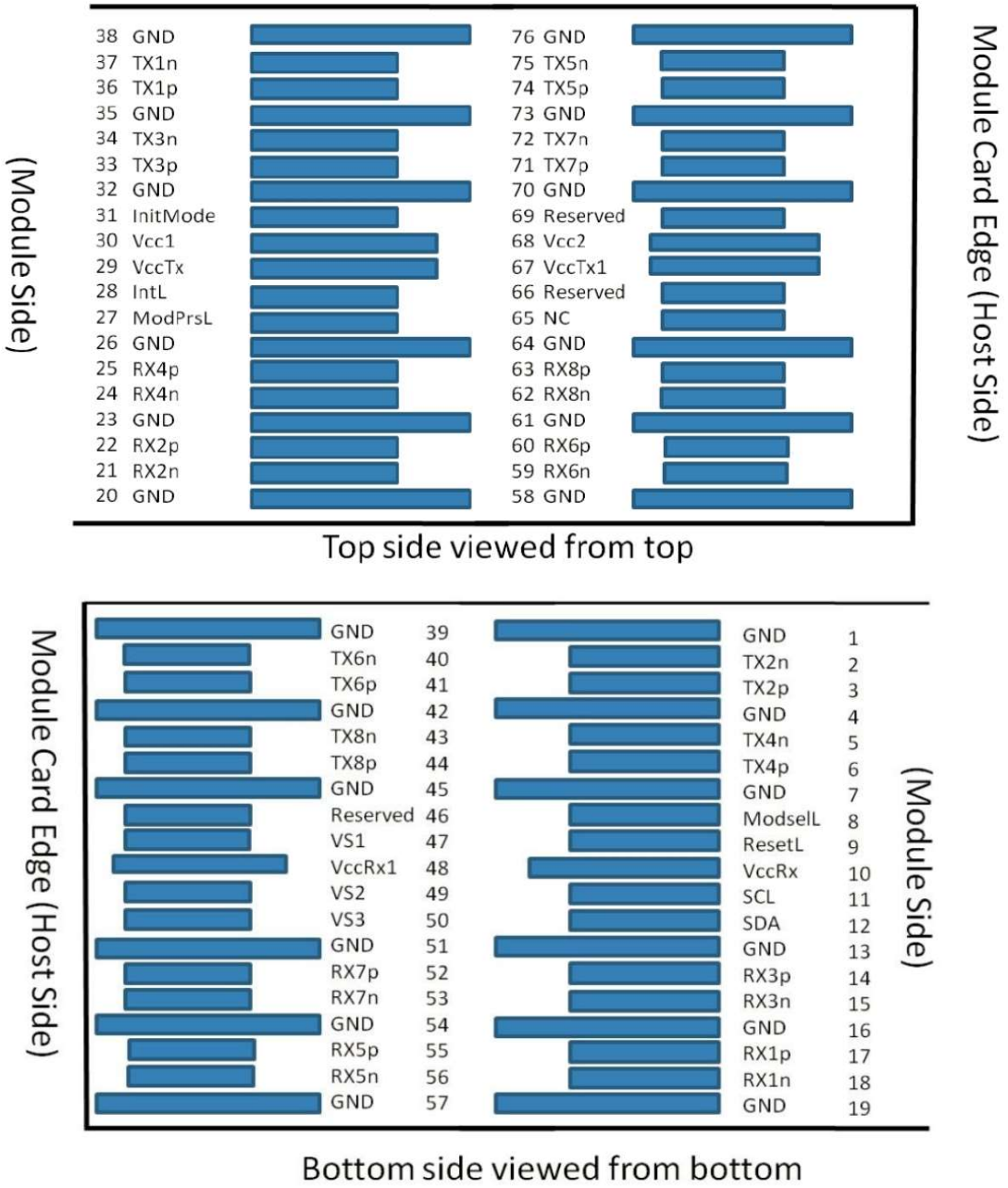


Figure 1-Pin definitions of the module high speed inputs/outputs

Pin Definitions

Pin #	Logic	Symbol	Definition
1		GND	Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRx	+3.3 V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-wire serial interface clock
12	LVCMOS-I/O	SDA	2-wire serial interface data
13		GND	Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Ground
20		GND	Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output

23		GND	Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29		VccTx	+3.3V Power supply transmitter
30		Vcc1	+3.3V Power supply
31	LVTTL-I	InitMode	Initialization mode
32		GND	Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Ground
39		GND	Ground
40	CML-I	Tx6n	Transmitter Inverted Data Input
41	CML-I	Tx6p	Transmitter Non-Inverted Data Output
42		GND	Ground
43	CML-I	Tx8n	Transmitter Inverted Data Input
44	CML-I	Tx8p	Transmitter Non-Inverted Data Output

45		GND	Ground
46		Reserved	
47		VS1	Module Vendor Specific 1
48		VccRx1	3.3V Power Supply
49		VS2	Module Vendor Specific 2
50		VS3	Module Vendor Specific 3
51		GND	Ground
52	CML-O	Rx7p	Receiver Non-Inverted Data Output
53	CML-O	Rx7n	Receiver Inverted Data Output
54		GND	Ground
55	CML-O	Rx5p	Receiver Non-Inverted Data Output
56	CML-O	Rx5n	Receiver Inverted Data Output
57		GND	Ground
58		GND	Ground
59	CML-O	Rx6n	Receiver Inverted Data Output
60	CML-O	Rx6p	Receiver Non-Inverted Data Output
61		GND	Ground
62	CML-O	Rx8n	Receiver Inverted Data Output
63	CML-O	Rx8p	Receiver Non-Inverted Data Output
64		GND	Ground
65		NC	No Connected

66		Reseved	
67		VccTx1	3.3V Power Supply
68		Vcc2	3.3V Power Supply
69		Reseved	
70		GND	Ground
71	CML-I	Tx7p	Transmitter Non-Inverted Data Output
72	CML-I	Tx7n	Transmitter Inverted Data Output
73		GND	Ground
74	CML-I	Tx5p	Transmitter Non-Inverted Data Output
75	CML-I	Tx5n	Transmitter Inverted Data Output
76		GND	Ground

Recommended QSFP-DD Host Board Schematic

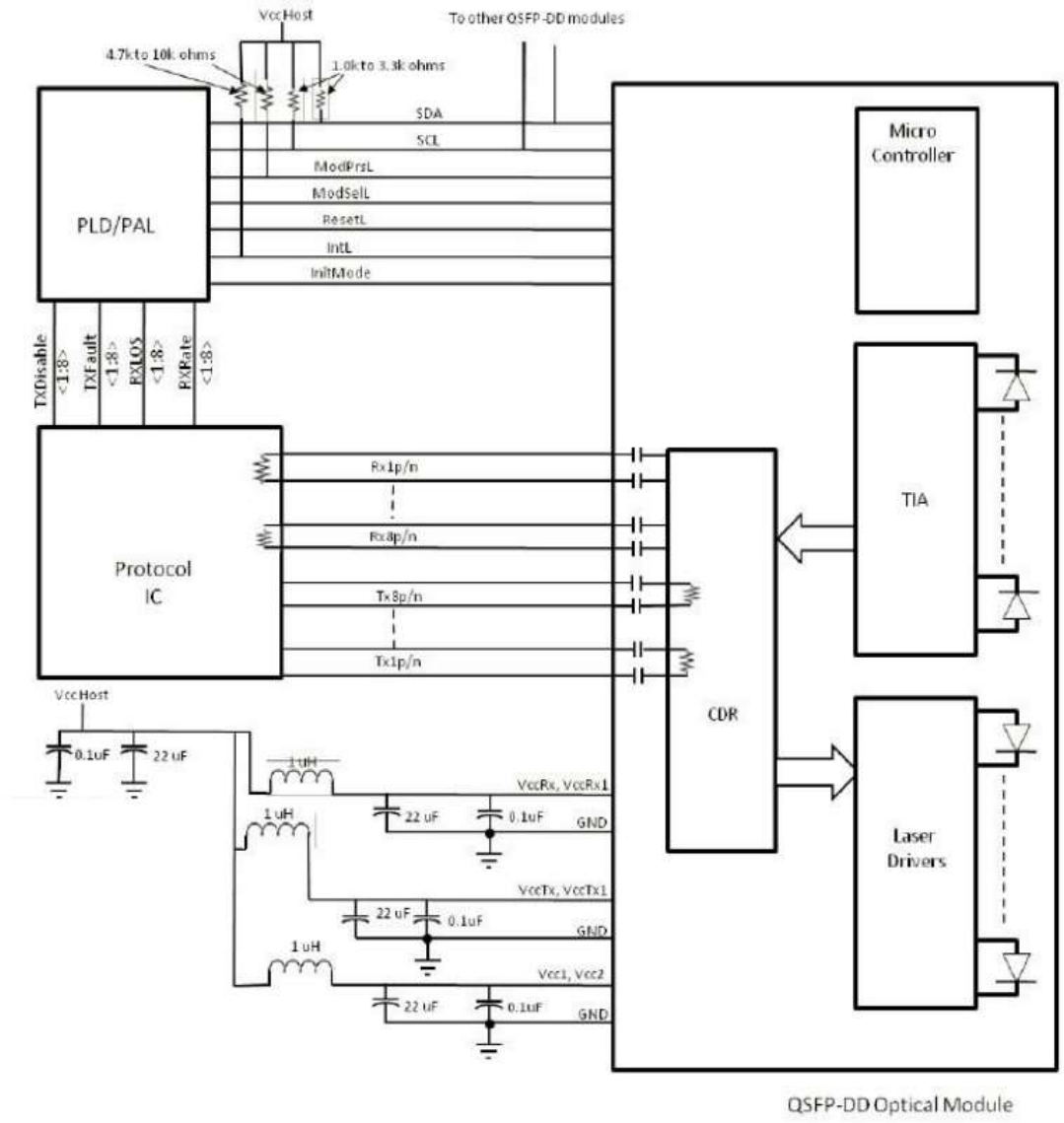
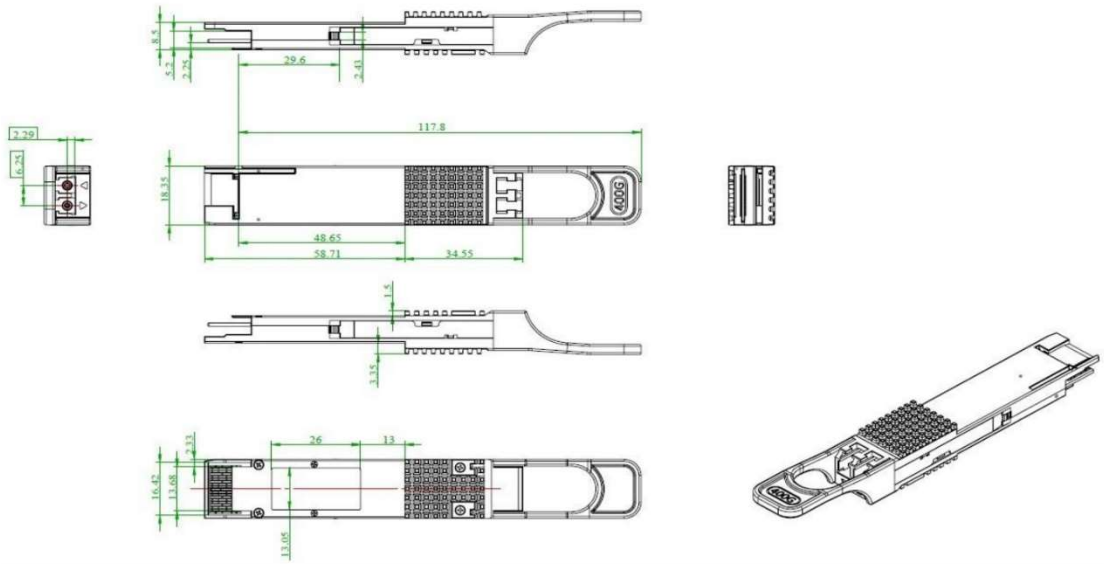


Figure 2-Recommended QSFP-DD Host Board Schematic

Notes:

1. Filter capacitor values are informative and vary depending on applications, 0.1 uF capacitors should be placed in close proximity to power pins and may be duplicated for individual pins to provide additional high frequency filtering.
2. Vcc1 and/or Vcc2 may be connected to VccTx, VccTx1 or VccRx, VccRx1 provided the applicable derating of the maximum current limit is used.

Mechanical Diagram



Order information

Part Number	Description
AE-QSFPDD-LR8	QSFP-DD 400GBASE LR8 1310nm 10km Transceiver